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				Application Number	10/650,445
				Filing Date	8/28/2003
				First Named Inventor	Lin, et al.
				Art Unit	2811
				Examiner Name	TBD
				Attorney Docket Number	TSM02-1369
Sheet	1	of	1		

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. <sup>1</sup>	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number - Kind Code <sup>2</sup> (if known)			
ON	1	US-4,998,510	03-12-1991	Rognon	
ON	2	US-6,137,149	10-24-2000	Kodama	
ON	3	US-6,420,218 B1	07-16-2002	Yu	

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No. <sup>1</sup>	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T <sup>6</sup>
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ON	4	Chau, R., et al., "A 50nm Depleted-Substrate CMOS Transistor (DST)," IEDM, pp. 621-624, 2001.	
ON	5	Choi, Y.K., et al., "Ultrathin-Body SOI MOSFET for Deep-Sub-Tenth Micron Era," IEEE Electron Device Letters, Vol. 21, No. 5, pp. 254-255, May 2000.	
ON	6	Yeo, Y.C., et al., "Design and Fabrication of 50-nm Thin-Body p-MOSFETs with a SiGe Heterostructure Channel," IEEE Transactions on Electron Devices, Vol. 49, No. 2, pp. 279-286, February 2002.	

Examiner Signature	ON	Date Considered	7/14/04
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